IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	
Ki-Young LEE, et al.	Examiner: Paul E. Brock II
Serial No. 09/389,491	Art Unit: 2815
Filed: September 3, 1999	
For: Semiconductor Integrated Circuit Capacitor and Method for Fabricating Same	Attorney Docket No.: 242/101

TRANSMITTAL OF APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA. 22313-1450

Sir:

This Appeal Brief is being filed in triplicate together with the fee as set forth in 1.17 (c) in the amount of $330.00 covering the appeal fee. The Commissioner of Patents is hereby authorized to charge the necessary fees to deposit account 5-01645.

Respectfully submitted,
LEE & STERBA, P.C.

Date: November 7, 2003

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

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APPELANT'S BRIEF UNDER 37 C.F.R. § 1.192

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INTRODUCTION

This is an appeal from the final rejection mailed on February 11, 2003, of claims 12, 14-24 and 26, all claims remaining in the above-identified patent application. These claims were rejected only under 35 U.S.C. § 103(a) as being unpatentable over two or three patent references.

REAL PARTY IN INTEREST

The real party in interest in the subject application is Samsung Electronics Co., LTD., to which the subject application is assigned.

RELATED APPEALS AND INTERFERENCES

There are no known appeals or interferences that will directly affect or be directly affected by or have a bearing on the decision of the Board of Patent Appeals and Interferences in the present appeal.

CLAIM STATUS

Twenty-six (26) original claims were filed in the subject application on September 3, 1999. Claims 12–26 were elected for prosecution in response to a Restriction Requirement mailed by the Office on December 15, 2000. In an Amendment filed on May 25, 2001, claims 1-11 and 25 were canceled as being directed to a non-elected group. Claim 13 was canceled in an Amendment filed on February 27, 2002, and the subject matter thereof was incorporated into claim 12. Presently, claims 12, 14-24 and 26 are pending, and are the appealed claims.

STATUS OF AMENDMENTS

An Amendment after Final Rejection, filed on May 12, 2003, was entered. In a subsequent Advisory Action, the Examiner reasserted a prior rejection of claims 12, 14-24 and 26.

SUMMARY OF INVENTION

The present invention relates to a capacitor having a metal insulator metal (MIM) structure, which can be used in a logic circuit or an analog circuit, and fabrication methods of making such MIM capacitors.

In a conventional processing method for fabricating a capacitor having a MIM structure useful in a conventional logic circuit or an analog circuit, a conductive layer is formed on an insulating substrate 100 and etched to form a lower electrode 102a and a first wire line 102b, as illustrated in FIG. 1 of the subject application. A planarized interlevel insulating layer 104 is formed on the insulating substrate 100 having the lower electrode 102a and the first wire line 102b, and a first via hole h1 is formed by selectively

etching the planarized interlevel insulating layer 104 to expose a predetermined portion of the surface of the lower electrode 102a, as illustrated in FIG. 2. A dielectric layer 106 is then formed on the interlevel insulating layer 104 and in the first via hole h1 by CVD. A second via hole h2 is formed in the insulating layer 104 by selectively etching the dielectric layer 106 and the interlevel insulating layer 104 to expose a predetermined surface of the first wire line 102b, as shown in FIG. 3. The second via hole h2 is typically narrower in width than the first via hole h1, as may be seen in FIG. 3. A conductive plug 108, typically including tungsten (W), is selectively formed in the second via hole h2 only, and a conductive layer such as an aluminum alloy layer is formed on the resultant surface and etched to define a capacitor formation part (102a/106/110a) and a wire line formation part (102b/108/110b) including a simultaneously formed second wire line 110b and upper electrode 110a, as illustrated in FIG. 4.

When etching the interlevel insulating layer 104 for forming the first via hole h1, a part of the lower electrode 102a is also etched, causing generation of a groove in part of the lower electrode 102a on the external lower side of the first via hole h1. Then, when the dielectric layer 106 is deposited, the groove may be imperfectly filled, thus causing a disconnection inferiority of the dielectric layer, or a "dielectric disconnection," illustrated by regions A in FIG. 5. If such a dielectric disconnection occurs, the circuit cannot have a uniform capacitance because of power leakage, and characteristic properties of the capacitor are decreased.

The present invention as claimed in independent claim 12 addresses this problem of dielectric disconnection with a method of manufacturing a semiconductor integrated circuit capacitor, in which first and second via holes h1 and h2 are simultaneously formed in an interlevel insulating layer 204 on an insulating substrate 200 in which a first wire line 202b and a lower electrode 202a are formed, so that a predetermined surface of the lower electrode 202a and a predetermined surface of the first wire line 202b are exposed by the first and second via holes h1 and h2, respectively, as illustrated in FIGS. 6 and 7. Then, a tungsten containing conductive layer 206 is formed on the interlevel insulating layer 204 and in the first and second via holes h1 and h2, including on the exposed

predetermined surfaces of the lower electrode 202a and first wire line 202b, as illustrated in FIG. 8.

The tungsten containing conductive layer 206 is then selectively etched back by a tungsten etch back process to simultaneously form: (i) a tungsten containing conductive sidewall spacer 208 on the sidewalls of the first via hole h1 and a portion of the exposed predetermined surface of the lower electrode 202a from the tungsten containing conductive layer formed in the first via hole h1 for preventing dielectric disconnection in lower corners of the first via hole h1; (ii) a tungsten containing conductive plug 210 in the second via hole h2 on the predetermined surface of the first wire line 202b from the tungsten containing conductive layer formed in the second via hole h2, the tungsten containing conductive sidewall spacer 208 and the tungsten containing conductive plug 210 being formed of the same tungsten containing conductive layer; and (iii) an exposed surface containing the spacer 208, conductive plug 210, a portion of the predetermined surface of the lower electrode 202a not covered by the tungsten containing conductive sidewall spacer 208, and predetermined surfaces of the interlevel insulating layer 204, as illustrated in FIG. 9. A dielectric layer 212 is then formed on the exposed surface, the tungsten containing conductive sidewall spacer 208 and the tungsten containing conductive layer formed in the first via hole, as further illustrated in FIG. 9.

The dielectric layer 212 is removed from the exposed surface except for a predetermined portion of the dielectric layer 212 disposed on the tungsten containing conductive sidewall spacer 208, and predetermined surface of the lower electrode 202a not covered by the tungsten containing conductive sidewall spacer 208. Finally, a second wire line 214b, connected to the tungsten containing conductive plug 208, and an upper electrode 214a, connected to the dielectric layer 212, are simultaneously formed, as illustrated in FIG. 10. *See U.S. Patent Application Serial No. 09/389,491, at p. 9, line 4 – p. 13, line 3.*

By forming the tungsten containing conductive sidewall spacer 208 in the first via hole h1 prior to depositing the dielectric layer thereon, the problem of dielectric disconnection at bottom corners of the first vial hole h1 is prevented, and characteristics of the capacitor are improved. *U.S. Patent Application Serial No. 09/389,491, at p. 13, lines 4-9.*

The remaining dependent claims, viz. claims 14-24 and 26, are dependent from claim 12, and include further limitations regarding the method of manufacturing the semiconductor integrated circuit capacitor, including materials by which the layers are formed, deposition methods of the layers, and a further limitation that the spacer formed on the sidewalls of the via hole has a sloping surface.

ISSUES

1. Rejection of claims 12, 14-16, 18-22, 24 and 26 under 35 U.S.C. § 103(a)
   A. The Gambino et al. reference does not address the problem of dielectric disconnection as described in the subject application.
   B. The nature of the Kuwajima reference precludes any teaching of a dielectric disconnection therein. The sidewall spacers of the Kuwajima reference are not equivalent to those of the present invention as claimed.
   C. Improper combination of prior art references and improper hindsight reconstruction.
2. Rejection of claim 17 under 35 U.S.C. § 103(a)
3. Rejection of claim 23 under 35 U.S.C. § 103(a)

GROUPING OF CLAIMS

Claims 12, 14-24 and 26 stand or fall together.

ARGUMENTS

1. Asserted Rejection of Claims 12, 14-16, 18-22, 24 and 26 Under 35 U.S.C. § 103(a)

In the Final Office Action mailed February 11, 2003, the Examiner rejected claims 12, 14-16, 18-22, 24 and 26 under 35 U.S.C. § 103(a) as being unpatentable over United States Patent No. 6,166,423 to Gambino et al. ("the Gambino et al. reference") in view of United States Patent No. 5,534,461 to Kuwajima ("the Kuwajima reference").

A. The Gambino et al. Reference

In the embodiment illustrated by FIGS. 11-20 of the Gambino et al. reference, which was cited against claims 12, 14-22, 24 and 26 in all six (6) Office Actions issued in the subject application, the Gambino et al. reference teaches a method of forming an integrated circuit having a capacitor in which two conductive interconnects 310 and 315 are formed on a first interlevel dielectric 305 by etching or a damascene process, and a second interlevel dielectric 307 is deposited upon the first interlevel dielectric 305 and upon the first and second conductive interconnects 310, 315 as illustrated in FIG. 11. A first opening 320 and at least one second opening 330 that extend down to the first and second conductive interconnects 310, 315 respectively, are formed in the second interlevel dielectric 305, as illustrated in FIG. 12. A layer of a third conductor 328, which may be a tungsten containing layer, is deposited on the second interlevel dielectric 305 to a thickness that the second opening 330 is filled with the third conductor 328, and the first opening 320 is not planarized by the third conductor 328, as illustrated in FIG. 13. Then, as illustrated in FIG. 14, the third conductor 328 is entirely removed from inside the first opening 320. An insulator 322 is formed on the first conductive interconnect 310 at the bottom of the first opening 320, on the second interlevel dielectric 307, on the third conductor 328, and in the second opening 330 preferably by a highly conformal method such as CVD or PECVD, "to ensure adequate coverage of the bottom of the first opening 320," as stated at col. 8 lines 3-11, and illustrated in FIG. 15 of the

Gambino et al. reference. A conductor 324 is later formed in the first opening 320, as illustrated in FIG. 17. *See the Gambino et al. reference at col. 7, line 39 - col. 8, line 11.*

The Gambino et al. reference teaches complete removal of the conductive layer 328 from inside the first opening 320 prior to deposition of the insulating layer 322 therein. The Gambino et al. reference further teaches achieving adequate coverage of the bottom of the first opening 320 by using CVD or PECVD to deposit the insulating layer 322 therein, thereby precluding a step coverage problem in the first opening 320. The Gambino et al. reference addresses neither a problem of dielectric disconnection as described in the subject application nor a problem of step coverage in the first opening 320. The Gambino et al. reference does, however, address a "conductor filling problem" that may occur in the second opening 330, which is entirely filled with the tungsten layer 328, and from which the tungsten layer 328 is not removed. *See the Gambino et al. reference at col. 7, lines 3-5.*

B. The Kuwajima Reference

The Kuwajima reference does not teach, mention or suggest the problem of dielectric disconnection that is addressed by the claims of present invention, and is in fact directed to an entirely different problem, namely that of obtaining a planarized wiring layer in a device having contact holes of differing diameters, and therefore differing aspect ratios. As a solution, the Kuwajima reference proposes to reduce the step or aspect ratio of a contact hole having a large diameter, while burying contact holes having smaller diameters.

To this end, the Kuwajima reference teaches forming a p-well in an n-type silicon substrate, forming field oxide regions surrounding an active region of the substrate in which a transistor is formed, and forming contact holes in an insulating film 12 formed on the silicon substrate having the transistor formed therein. The contact holes are for source/drain regions and a well region, the contact hole for the well region having a larger diameter than that of the contact holes of the source/drain regions.

The Kuwajima reference teaches depositing barrier metal layers 13a and 13b of Ti and/or TiN on the substrate and in the contact holes as illustrated in FIGS. 3 and 4 of the of the same. Thereafter, a tungsten layer 14 is deposited on the substrate and in the

contact holes having the barrier metal layers 13a and 13b thereon. The tungsten is removed from the insulating film near the contact holes and from a flat bottom portion of the contact hole for the well region, so that a tapered portion of the tungsten 14c remains on the sidewalls of the large contact hole for the well region, thereby reducing the step of the contact hole for the well regions. The tungsten 14c remaining in the contact hole is formed entirely on the barrier metal layers 13a and 13b, and not on the insulating material of the sidewalls of the contact hole.

Thereafter, a wiring layer 16 is deposited on the surface of the substrate by Al or Al alloy sputtering such that the contact hole for the well region is filled with the wiring layer, as illustrated in FIG. 5, which is then patterned as illustrated in FIG. 6. *See the Kuwajima reference at col. 3, line 12 – col. 5, line 43.*

At no time is a dielectric layer formed in or on the contact holes of the Kuwajima reference. Therefore, as previously submitted, a problem of dielectric disconnection does not exist in the Kuwajima reference, and any teaching directed toward a problem of dielectric disconnection in the Kuwajima reference is precluded by the very nature of the reference itself.[1]

Further, with the exception of a gate electrode 5 at col. 3, lines 30-35, the Kuwajima reference does not teach formation of any electrode, including a lower electrode for a capacitor.

Not withstanding the teachings of the prior art references, in rejecting claims 12, 14-16, 18-22, 24 and 26 in the Final Rejection mailed on February 11, 2003, the Examiner asserts that the Kuwajima reference teaches performing a tungsten etch back process to form:

> a tungsten containing conductive sidewall spacer on sidewalls of the first via hole and a portion of an exposed predetermined surface of **a lower electrode (13b** left of center in via 15c) from the tungsten containing conductive layer formed in the first via hole **for preventing dielectric disconnection**; ii) a tungsten containing conductive plug in the second via hole on the predetermined surface of **a first wire line (13b** above right most region 8).

[1] See the Amendments filed by Applicants on 12-12-02 and 5-12-03.

Office Action of February 11, 2003, at p. 3 (emphasis added).

However, as stated in the Kuwajima reference at col. 4, lines 9-11 and illustrated in FIG. 3 of the same, the TiN layer 13b is a barrier metal layer, not an electrode.

Furthermore, Applicants have repeatedly argued that the assertion made by the Examiner that the tungsten etch back process and structures resulting therefrom are "for preventing dielectric disconnection" in the Kuwajima reference is inherently flawed, as there is no dielectric in the contact holes of the Kuwajima reference in which dielectric disconnection could occur, making the prevention thereof a moot point.[1]

Therefore, an assertion of preventing such dielectric disconnection in the Kuwajima reference is groundless.

It has also been submitted that although the Kuwajima reference discloses tungsten sidewall spacers *per se*, these tungsten sidewall spacers are left in a trench to improve the step coverage of a wiring layer to be deposited in the trench, and further, these tungsten sidewall spacers are deposited entirely on the barrier metal layer, and not on the insulating sidewalls of the contact hole. The purpose, function, result and manner of use of the tungsten sidewall spacers according to the Kuwajima reference is completely different from the purpose, function, result and manner of use of the sidewall spacers of the present invention that addresses the problem of possibly incurring dielectric disconnection in a dielectric layer that is deposited on an electrode in a via hole, which problem is not possible in the Kuwajima reference.[1]

Despite these arguments as supported by the prior art, the Examiner insists on mischaracterizing the teachings of the prior art by simply asserting that the mere presence of tungsten sidewall spacers in the Kuwajima reference is sufficient teaching and suggestion to use the sidewall spacers in the present invention. This assertion is tantamount to saying that the mere teaching of a sidewall spacer in a reference for a particular purpose or function precludes the patentability of an entirely different method, which also utilizes a sidewall spacer albeit for an entirely different purpose and function.

[1] See the Amendments filed by Applicants on 12-12-02 and 5-12-03.

C. Improper Combination of Prior Art References and Improper Hindsight Reconstruction

It is not enough that one may modify a reference in view of a second reference, but rather it is required that the second reference suggest the modification of the first reference, and not merely provide the capability of modifying the first reference.

In view of the teachings of the prior art references, particularly the complete lack of a dielectric layer in which to incur a dielectric disconnection in the contact holes of the Kuwajima reference, and the lack of reference to a dielectric disconnection problem or a step coverage problem in the first opening of the Gambino et al. reference, Applicants have repeatedly submitted that there is no motivation to combine the tungsten sidewall spacers taught in the Kuwajima reference with the device of the Gambino et al. reference, and that any combination thereof to reject the claims of the subject application is improper and based on impermissible hindsight construction.[1]

It is well-settled law that for a claimed invention to be rejected on grounds of obviousness, the prior art must suggest the modifications sought to be patented. *See In re Gordon*, 221 USPQ 1125, 1127 (Fed. Cir. 1984); *see also ACS Hospital Systems, Inc. v. Montefiore Hospital*, 221 USPQ 929, 933 (Fed. Cir. 1984). In fact, the United States Court of Appeals for the Federal Circuit ("Federal Circuit") has stated: "[w]hen determining the patentability of a claimed invention which combines two known elements, 'the question is whether there is something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination.'" *In re Beattie*, 24 USPQ2d 1040, 1042 (Fed. Cir. 1992) (quoting *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 488 (Fed. Cir. 1984)).

This teaching, suggestion or motivation to combine "may flow from the prior art references themselves, the knowledge of one of ordinary skill in the art, or, in some cases, from the nature of the problem to be solved." *In re Dembiczak*, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999), *abrogated on other grounds* by *In re Gartside*, 53 USPQ2d 1769 (Fed. Cir. 2000). While the law does not require that the references must expressly teach

[1] See the Amendments filed by Applicants on 12-12-02 and 5-12-03.

that the disclosure contained in one should be combined with the disclosure of another, the showing of combinability of the references must be "clear and particular." *Id.* In the instant application, however, there is no suggestion or motivation for the proposed combinations of the art relied upon by the Examiner. Accordingly, any combination of the art without such evidence is an improper hindsight reconstruction using applicant's invention as a template. *See id.*

However, the Examiner has maintained the rejections, and in the Advisory Action mailed on May 29, 2003, the Examiner states:

> [I]n response to applicant's argument that "it is not understood how one of skill in the art would interpret and apply a tungsten sidewall spacer left in a trench to improve step coverage of a wiring layer to the completely unrelated problem of the possibility of dielectric disconnection," a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See In re Casey, 152 USPQ 235 (CCPA 1967) and In re Otto, 136 USPQ 458, 459 (CCPA 1963). **In this case, the tungsten sidewall spacer is intended to be used to prevent dielectric disconnection.** Therefore the applicant's arguments are not persuasive, and the rejection is proper.

Advisory Action of May 29, 2003, at p. 2 (emphasis added).

However, it is respectfully submitted that the Examiner's repeated assertion that "the tungsten sidewall spacer is intended to be used to prevent dielectric disconnection" is necessarily based on improper hindsight reconstruction, because, as has been previously argued, the tungsten sidewall spacer of the Kuwajima reference is formed on a barrier metal layer and a metal wiring layer is formed on the tungsten sidewall spacer.[1,2] There is no dielectric layer formed on the tungsten sidewall spacer of the Kuwajima

[1] See the Amendments filed by Applicants on 12-12-02 and 5-12-03.

[2] See the Office Action of September 16, 2002, and the Office Action made Final of February 11, 2003.

reference. Accordingly, there is absolutely no possibility of dielectric disconnection in the Kuwajima reference. Therefore, the tungsten sidewall spacer cannot be intended to be used to prevent dielectric disconnection as asserted by the Examiner, and in fact, the Kuwajima reference itself teaches that the sidewall spacer 14c, which is formed on the barrier metal layer 13b, and not on the insulating material 12 in which the contact hole is formed, is for improving the step coverage of a wiring layer.

Despite Applicants' repeated arguments to the effect presented above, in the Advisory Action mailed on May 29, 2003, the Examiner also states:

> [I]n response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See In re McLaughlin, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Advisory Action of May 29, 2003, at p. 2.

However, by asserting that the barrier metal layer 13b of the Kuwajima reference is an electrode, and that the sidewall spacers 14c of the Kuwajima reference are for preventing dielectric disconnection, it is respectfully submitted that the Examiner is taking structural features of the prior art that appear visually similar to those of the subject application out of the context of the prior art reference, thereby divorcing from the structure the function or purpose of that structure as taught by that reference, and then mentally attaching to the structure a new and completely different function or purpose as taught by the subject application, which is not taught in the prior art, and using such teaching to reconstruct the claims of the present invention just to reach the rejection thereof.

Specifically, the Examiner took the tapered tungsten sidewall spacer 14c out of the context of the Kuwajima reference, in which its purpose is to improve the step coverage of the contact hole and in which it is formed on the barrier metal layer 13b only and not on the insulating material of the sidewalls of the contact hole, and applied to the

tapered tungsten sidewall spacer 14c functions taught in the subject application, which are not taught in the prior art references, and which are precluded in the Kuwajima reference by the very nature of the Kuwajima reference, to reverse engineer the claims of the subject application based on the teachings thereof.

Accordingly, it is respectfully submitted that based on the teachings of the cited prior art references, the Examiner's conclusion of obviousness necessarily includes knowledge gleaned only from the applicant's disclosure, and such a reconstruction is in fact improper.

Therefore, claims 12, 14-16, 18-22, 24 and 26 are believed to be patentably distinguished over the cited prior art references and in condition for allowance.

Accordingly, favorable action by the Board on claims 12, 14-16, 18-22, 24 and 26 is respectfully requested.

2. Rejection of claim 17 under 35 U.S.C. § 103(a)

In the Final Office Action mailed February 11, 2003, the Examiner rejected claim 17 under 35 U.S.C. § 103(a) as being unpatentable over the Gambino et al. reference and the Kuwajima reference as applied to claims 12 and 14, and further in view of United States Patent No. 6,074,907 to Oh et al. ("the Oh et al. reference"). Applicants have previously submitted that that there is no motivation or basis to combine the teachings of the Gambino et al. reference and the Kuwajima reference to arrive at this rejection other than through impermissible hindsight construction, and that combining the teachings of the Oh reference with those of the Kuwajima reference and the Gambino et al. reference does not render claim 17 of the subject application obvious, as the combined teachings do not teach all the limitations of claim 12, from which claim 17 indirectly depends.[1]

Accordingly, the rejection of claim 17 is traversed, and favorable action by the Board on claim 17 is respectfully requested.

3. Rejection of claim 23 under 35 U.S.C. § 103(a)

In the Final Office Action mailed February 11, 2003, the Examiner rejected claim 23 under 35 U.S.C. § 103(a) as being unpatentable over the Gambino et al. reference and the Kuwajima reference as applied to claim 12, and further in view of United States Patent No. 6,066,555 to Nulty et al. ("the Nulty et al. reference").

Applicants have submitted that there is no motivation or basis to combine the teachings of the Gambino et al. reference and the Kuwajima reference to arrive at this rejection other than through impermissible hindsight construction, and that combining the teachings of the Nulty et al. reference with the teachings of the Gambino et al. reference and/or the Kuwajima reference does not render claim 23 of the subject application obvious, as the combined teachings do not teach all the limitations of claim 12, from which claim 23 depends.[1]

Accordingly, the rejection of claim 23 is traversed, and favorable action by the Board on claim 23 is respectfully requested.

Applicants submit that claims 12, 14-24 and 26 are in condition for allowance, and a notice to such effect is respectfully requested.

Respectfully submitted,

LEE & STERBA, P.C.

Date: November 7, 2003

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[1] See the Amendments filed by Applicants on 12-12-02 and 5-12-03.